REMARKS

Applicant filed a Notice of Appeal for the above-identified application in response to the Office Action dated July 3, 3002. The Notice of Appeal was mailed to the Office by applicant on December 3, 2002 and was apparently entered by the Office on December 12, 2002. Applicant is filing this Amendment together with a Request for Continued Examination. Applicant has amended claims 13, 15-16, 30 and 33, canceled claims 14, 26-29 and 31 without prejudice, and added new claims 34-39. Claims 13, 15-19, 30 and 32-39 are currently pending. Reexamination and reconsideration are respectfully requested.

The rejections of claims 14, 26-29 and 31 have been rendered moot at this time as these claims have been canceled without prejudice.

Claims 13, 16, 30 and 32-33 were rejected under 35 U.S.C. 102(b) or 103(a) as unpatentable over Yamaguchi et al. (US 5,394,001). The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner has cited no portion of the art the describes or suggests all of the elements of claim 13, as amended, including, for example, "a groove formed in the semiconductor substrate at a position between the first and second memory cell areas." Accordingly, applicant respectfully submits that the rejection of claim 13 and its dependent claim 16 be withdrawn. Claims 30-33 can be distinguished at least in a similar manner as claim 13.

Applicant notes that claims 15 and 17-19 depend from claim 13 and are patentable for at least the same reasons as claim 13.

New claims 34-39 have been added. Support for the new claims may be found throughout the specification and drawings and in the original claims. It is believed that no new matter has been entered. Examination of the new claims is respectfully requested.

Attached hereto is a marked-up version of the claim amendments made by the present amendment. The attached page is captioned "Version with markings to show changes made."

With regards to the restricted claims, applicant did not intend to offend the Examiner in the previous response where applicant cited MPEP section 803 that states that "if the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions."

Applicant was merely requesting that the Examiner reconsider the second restriction requirement and offer a more detailed explanation to support the second restriction requirement.

Applicant respectfully submits that claims 13, 15-19, 30 and 32-39 are in condition for allowance. Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes — Feb. 12, 2003

Alan S. Raynes **(Date)**

Version With Markings to Show Changes Made

Claims 13, 15-16, 30 and 33 were amended as follows:

13. (twice amended) A semiconductor device comprising:

tunnel insulating films, floating gates, dielectric films and control gates, all of which are laminated on first and second cell areas on a semiconductor substrate;

sources and drains formed [on] in the first and second cell areas at positions in contact with a common plane defined by a surface of the semiconductor substrate;

a groove in the semiconductor substrate at a position between the first and second cell areas; and

a connecting area extending under the groove within the semiconductor substrate, the connecting area being capable of electrically connecting one of the source and drain of the first cell area with one of the source and drain of the second cell area, wherein the connecting area has an electric resistance which is lower than any one of the sources and drains of the first and second cell areas.

15. (amended) The semiconductor device according to claim 13 [14], wherein an impurity concentration of the connecting area is the same as an impurity concentration of one of the sources and drains of the first and second cell areas, and is higher than an impurity concentration of the other of the sources and drains of the first and second cell areas.

16. (amended) The semiconductor device according to claim 13 [14], wherein the impurity concentration of the connecting area is higher than the impurity concentrations of all the sources and drains of the first and second cell areas.

30. (amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first horizontal field effect transistor comprising a first tunnel insulating film in contact with the semiconductor substrate, a first floating gate in contact with the tunnel insulating film, a first dielectric layer in contact with the floating gate, a

first control gate in contact with the dielectric layer, and first source/drain regions extending into the semiconductor substrate;

the second memory cell area including a second horizontal field effect transistor comprising a second tunnel insulating film in contact with the semiconductor substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the semiconductor substrate;

the first source/drain regions and the second source/drain regions each including an upper surface that extends along a common plane;

a groove located in the semiconductor substrate at a position between the first and second memory cell areas; and

a connecting area capable of electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than any of the source/drain regions, wherein the connecting area extends under the groove in the semiconductor substrate.

33. (amended) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first field effect transistor comprising a first tunnel insulating film in contact with the substrate, a first floating gate in contact with the tunnel insulating film, a first dielectric layer in contact with the floating gate, a first control gate in contact with the dielectric layer, and first source/drain regions extending into the substrate;

the second memory cell area including a second field effect transistor comprising a second tunnel insulating film in contact with the substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the substrate;

a connecting area capable of electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the

second source/drain regions, and wherein the impurity concentration of the connecting area is higher than the impurity concentrations of the first source/drain regions and higher than the impurity concentrations of the second source/drain regions; and

a groove [formed on] in the substrate above at least a portion of the connecting area [of the substrate], wherein no portion of the floating gate is positioned within the groove.